features

- 3-Channel CMOS ADC
- Single 3.3-V Supply
- 8-Bit 30-MSPS A/D Conversion
- Very Low Power: <300 mW Typical
- Differential Linearity Error: < ±0.5 LSB Max
- Integral Linearity Error: < ±0.75 LSB Max
- Analog Input Voltage Range: 1 Vpp Max
- 64-Pin Thin QFP Package
- Analog Input Bandwidth: >130 MHz
- Selectable Clamping Function for YUV or RGB Applications
- High-Precision Clamp: ±0.5 LSB
- Selectable Output Data Format for 4:4:4 (RGB, YUV), 4:2:2 and 4:1:1 (YUV) Format
- NTSC or PAL Compliant

applications

- Digital TV
- Digital Video
- Multimedia
- Video Capture
- Video Editing
- Security Applications

description

The TLV5734 is a triple 8-bit converter with high-precision clamp for digitizing video signals in RGB or YUV color spaces. The device supports pixel rates up to 30 MSPS. The TLV5734 is powered from a single 3.3-V supply. Separate clamping levels are provided for the RGB and YUV analog component video inputs. The clamp timing window is provided by an external pulse. The output-data formatter selects from output formats of 4:4:4, 4:1:1, and 4:2:2. For RGB applications, the 4:4:4 output format with clamp can be used. The TLV5734 is characterized for operation from –20°C to 75°C.

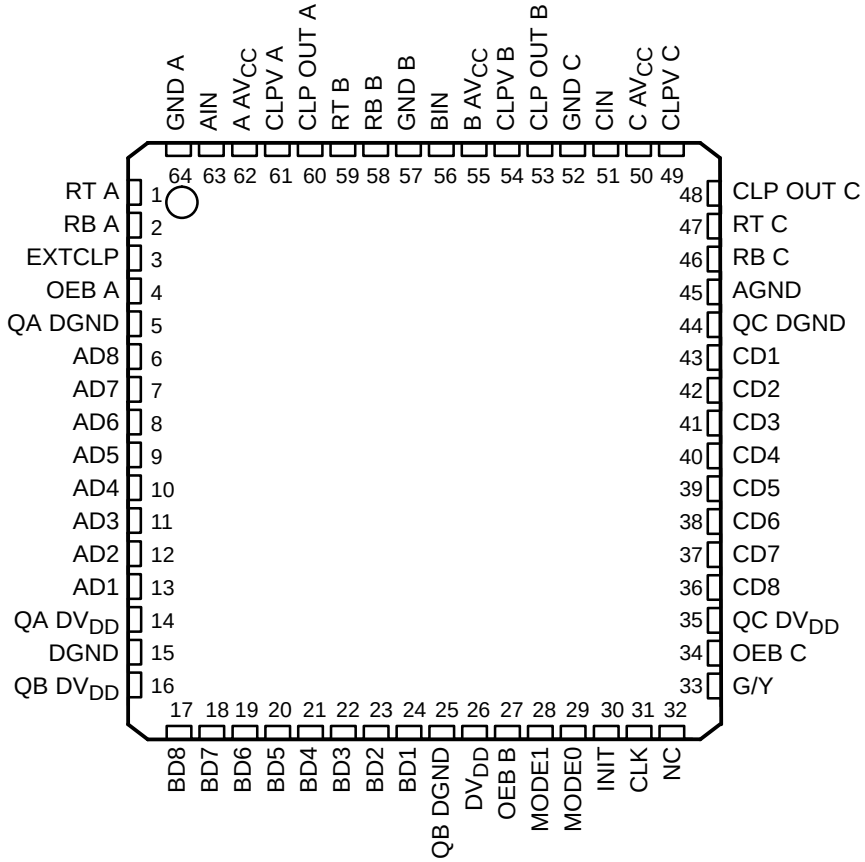
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	64-PIN THIN QUAD FLATPACK
–20°C to 75°C	TLV5734PAG

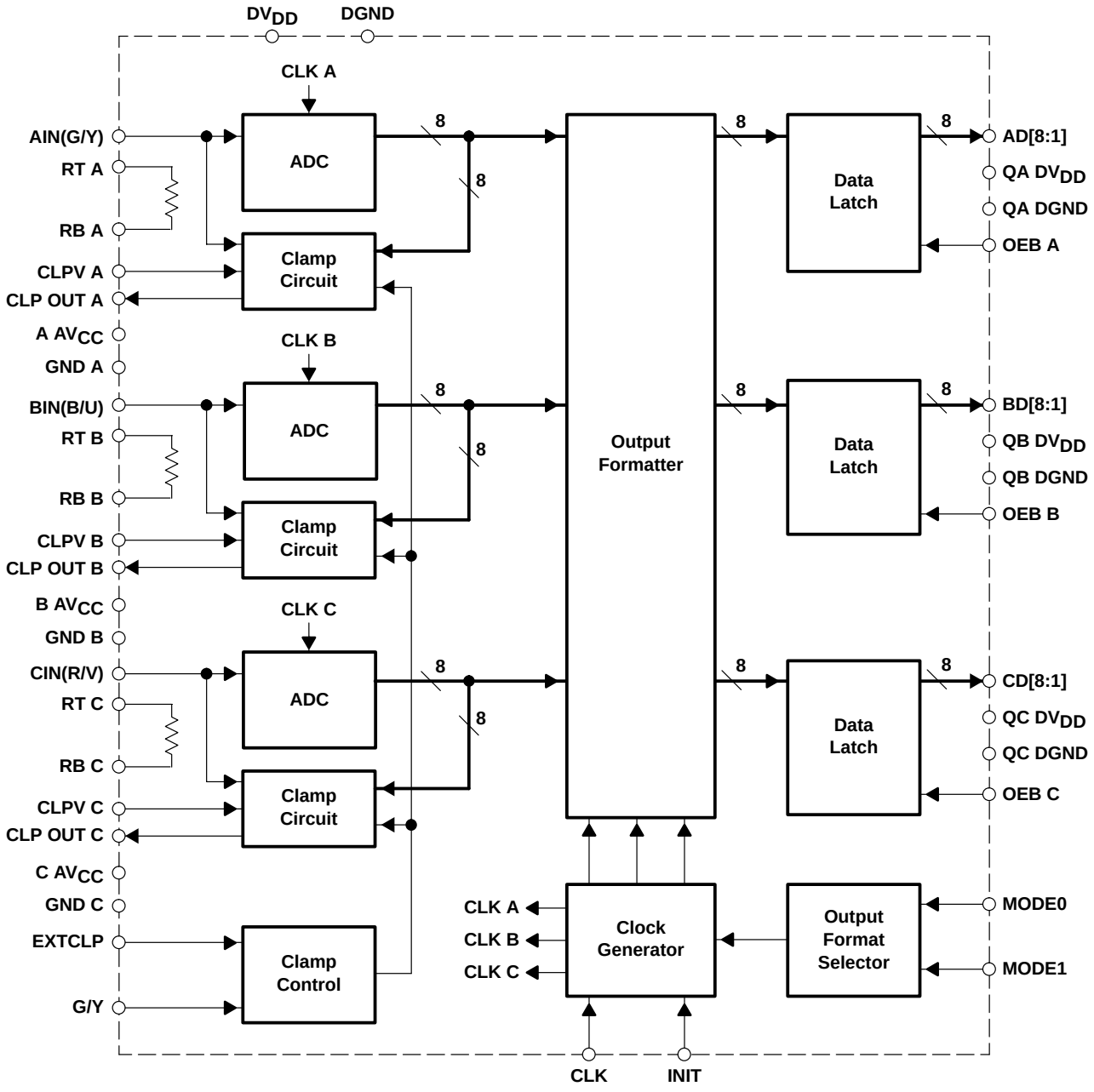
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

pin assignments

PAG PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	TYPE†	DESCRIPTION
A AV_{CC}	62	I	A	Analog supply (3.3 V) for ADC A
AD8–AD1	6–13	O	D	Data output of ADC A (MSB:AD8, LSB:AD1) (format 1, format 2, format 3)
AGND	45	I	A	Substrate ground
AIN	63	I	A	Analog input of ADC A. Used for G/Y
B AV_{CC}	55	I	A	Analog supply (3.3 V) for ADC B
BD8–BD1	17–24	O	D	Data output of ADC B (MSB:BD8, LSB:BD1) (format 2) Data output of ADC B, C (format 1, format 3)
BIN	56	I	A	Analog input of ADC B. Uses for B/U
C AV_{CC}	50	I	A	Analog supply (3.3 V) for ADC C
CD8–CD1	36–43	O	D	Data output of ADC C (MSB:CD8, LSB:CD1) (format 2) When MODE1 = L, MODE0 = L, CD8 outputs MSB flag of BD8–BD5 (format 1) When MODE1 = L, MODE0 = L, CD7 outputs LSB flag of BD8–BD5 (format 1) When MODE1 = H, MODE0 = L, CD8 outputs B channel flag of BD8–BD1 (format 3) When MODE1 = H, MODE0 = L, CD7 outputs B channel flag of BD8–BD1 (CD8–CD1) (format 3)
CIN	51	I	A	Analog input of ADC C. Used for R/V
CLK	31	I	D	Clock input. The clock frequency is four times the frequency subcarrier (fsc) for most video systems (see Table 3).
CLP OUT A	60	O	A	Clamp bias current of ADC A. A resistor-capacitor network sets the clamp settling time.
CLP OUT B	53	O	A	Clamp bias current of ADC B. A resistor-capacitor network sets the clamp settling time.
CLP OUT C	48	O	A	Clamp bias current of ADC C. A resistor-capacitor network sets the clamp settling time.
CLPV A	61	I	A	Clamp level of ADC A (see Table 1)
CLPV B	54	I	A	Clamp level of ADC B (see Table 1)
CLPV C	49	I	A	Clamp level of ADC C (see Table 1)
DGND	15	I	D	Digital ground for all logic
DV_{DD}‡	26	I	D	Digital supply (3.3 V) for all logic. DV_{DD}, QA DV_{DD}, QB DV_{DD}, and QC DV_{DD} are tied together internally.
EXTCLP	3	I	D	External clamp pulse input (active high)
GND A	64	I	A	Analog ground of ADC A
GND B	57	I	A	Analog ground of ADC B
GND C	52	I	A	Analog ground of ADC C
G/Y	33	I	D	Video input mode selector, low for RGB, high for YUV
INIT	30	I	D	Output initialized. The output data is synchronized with the first falling edge of CLK after INIT changes from low to high (see Figure 1). INIT is a control terminal that allows the external system to initialize the TLV5734 data conversion cycle.
MODE1,0	28,29	I	D	Output format mode selector (see Table 4)
NC	32	I	D	**NC should be tied low when using this device.**
OEB A	4	I	D	Output enable of ADC A (active low)
OEB B	27	I	D	Output enable of ADC B (active low)
OEB C	34	I	D	Output enable of ADC C (active low)
QA DGND	5	I	D	Digital ground for output driver of ADC A
QA DV_{DD}‡	14	I	D	Digital supply (3.3 V) for output driver of ADC A. DV_{DD}, QA DV_{DD}, QB DV_{DD}, and QC DV_{DD} are tied together internally.
QB DGND	25	I	D	Digital ground for output driver of ADC B

† A = analog pin, D = digital pin
‡ **These pins should be driven from the same power supply.**

Terminal Functions (Continued)

TERMINAL		I/O	TYPE†	DESCRIPTION
NAME	NO.			
QB DV_{DD}‡	16	I	D	Digital supply (3.3 V) for output driver of ADC B. DV_{DD}, QA DV_{DD}, QB DV_{DD}, and QC DV_{DD} are tied together internally.
QC DGND	44	I	D	Digital ground for output driver of ADC C
QC DV_{DD}‡	35	I	D	Digital supply (3.3 V) for output driver of ADC C. DV_{DD}, QA DV_{DD}, QB DV_{DD}, and QC DV_{DD} are tied together internally.
RB A	2	I	A	Bottom reference voltage level for ADC A
RB B	58	I	A	Bottom reference voltage level for ADC B
RB C	46	I	A	Bottom reference voltage level for ADC C
RT A	1	I	A	Top reference voltage level for ADC A (nominal RT A – RB A = 1 V for video signals)
RT B	59	I	A	Top reference voltage level for ADC B (nominal RT B – RB B = 1 V)
RT C	47	I	A	Top reference voltage level for ADC C (nominal RT C – RB C = 1 V)

† A = analog pin, D = digital pin

‡ **These pins should be driven from the same power supply.**

detailed description

ADC

The TLV5734 includes three 8-bit A/D channels. Each ADC employs a three-stage switched capacitor-pipelined architecture to achieve high accuracy and high throughput with low power consumption. The analog input is sampled when the external clock, CLK, goes from low to high. The INIT signal is used to initialize the order of output data when operating in the 4:2:2 or 4:1:1 output format mode. After INIT changes from low to high, the first reinitialized output data is available after a 5-clock-cycle delay from the rising edge of the CLK (see the timing diagram, Figure 1).

Pulling the OEB pin (pin 4, 27 or 34) high puts the corresponding ADC output in the high-impedance state.

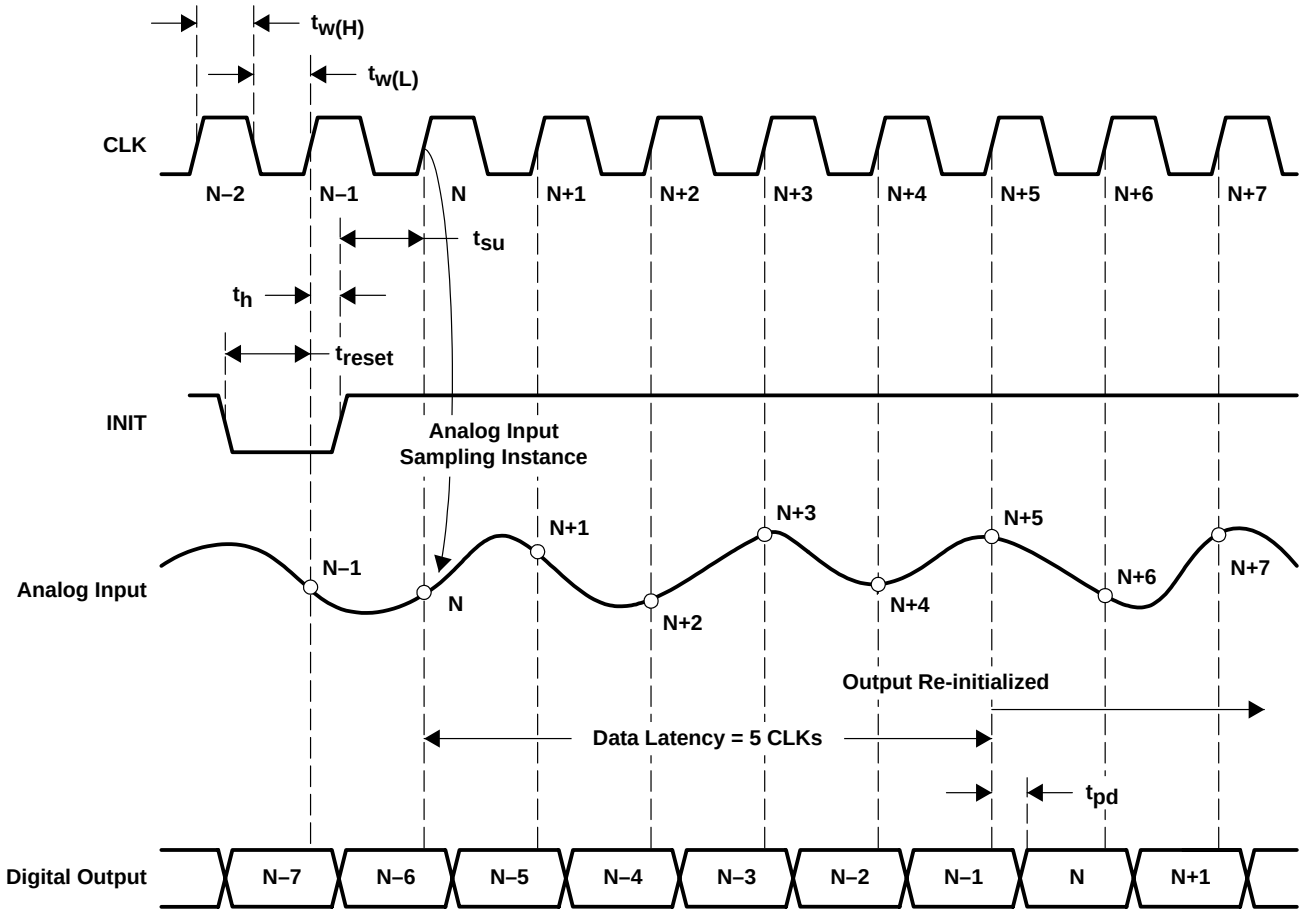


Figure 1. Timing Diagram

detailed description (continued)

clamp function

The TLV5734 employs a clamp feedback circuit on each channel to correct the clamp level mismatch contributed by the offset of each channel. The clamp levels are used for either the YUV or RGB video signal. Figure 2 shows the clamp circuit and the external R and C required for the clamp operation. The clamp circuit also requires an externally generated active-high clamp pulse to be applied to input EXTCLP. The clamp pulse defines the timing window during which the clamp circuit is enabled. For video applications, the clamp pulse must be applied during the back porch of the sync portion of the horizontal blanking interval. For an embedded sync video input (G/Y), the external clamp high must start after the gap A between sync and clamp start (see Figure 3 and Table 3).

The clamp is enabled by applying a logic high on the EXTCLP input. This closes switch SW1 and enables the digital comparator. The output of the ADC is then compared digitally with the preset clamp level (as defined in Table 1), then the voltage on clamp capacitor C2 is charged/discharged through the 3-state buffer and resistor R to make the ADC output equal to the desired clamp level. Once the desired clamp level is attained, the 3-state buffer is put in the high-impedance mode and the clamp voltage is stored on input capacitor C1 until the next clamp pulse.

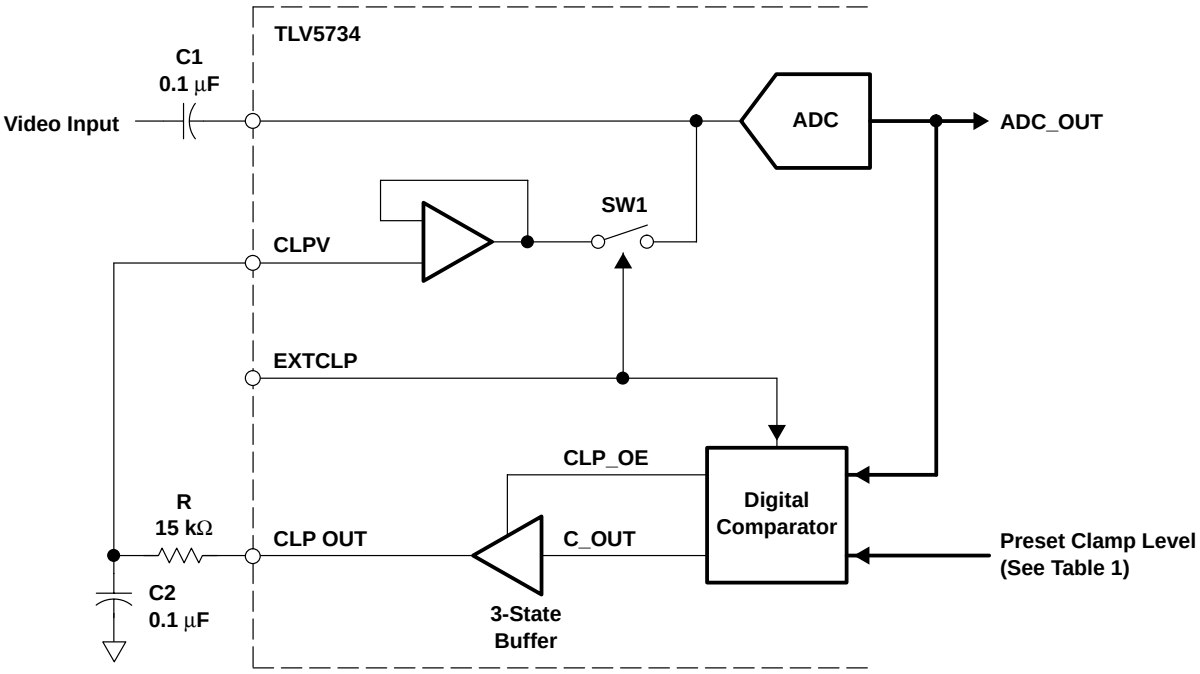


Figure 2. Clamp Feedback Circuit

Table 1. Preset Clamp Level

ADC CHANNEL	YUV (G/Y = HIGH)		RGB (G/Y = LOW)	
	OUTPUT CODE	APPLICATION	OUTPUT CODE	APPLICATION
CHANNEL A	00010000b	Y	00010000b	R, G, B
CHANNEL B	10000000b	U, V	00010000b	R, G, B
CHANNEL C	10000000b	U, V	00010000b	R, G, B

clamp function (continued)

Table 2. Clamp Operation

ADC_OUT	CLP_OE	CLP_OUT	BUFFER	RC
<REF	1	HIGH	H	Charge
= REF	0	HIGH	Z	Hold
> REF	1	LOW	L	Discharge

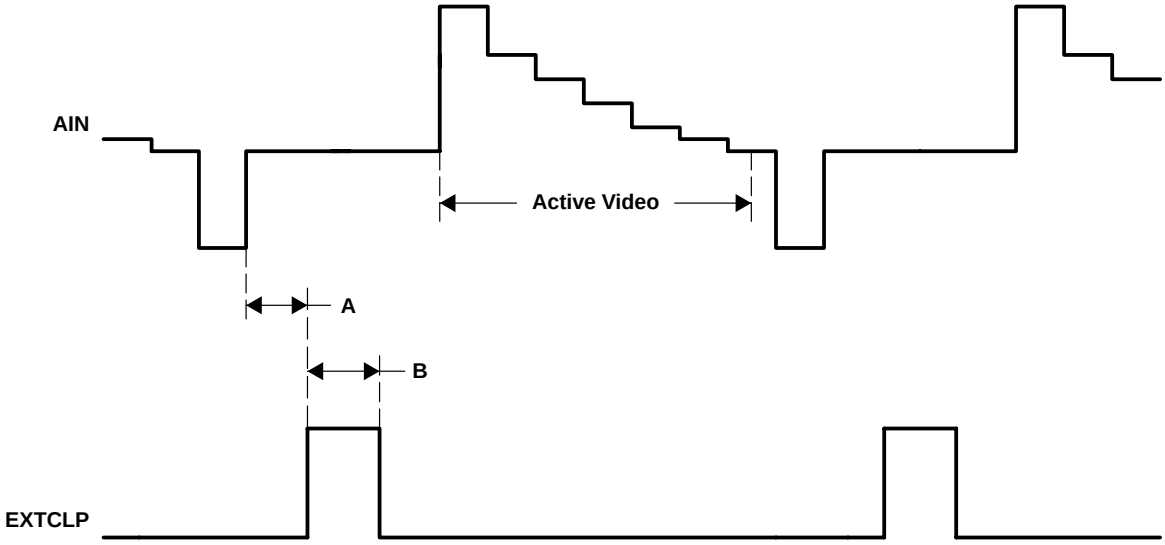


Figure 3. Clamp Timing Diagram

Table 3. Clamp Timing

TIME INTERVAL	NTSC 4fsc = 14.318 MHz	PAL 4fsc = 17.745 MHz	BT 601 × 2 = 27 MHz (NTSC)
A (Min.)	8 clocks (0.56 μs)	8 clocks (0.45 μs)	16 clocks (0.59 μs)
B (Min.)	16 clocks (1.12 μs)	16 clocks (0.90 μs)	32 clocks (1.19 μs)

output data format

The TLV5734 can select three output data formats for different video data processing by the combination of MODE0 and MODE1 (see Table 4). The output is synchronous with the rising edge of CLK that comes after INIT is pulled high. Timing diagrams and output data tables for formats 1, 2, and 3 are shown in Figure 4 through Figure 6 and Table 5 through Table 7.

Table 4. Output Data Format Selection

CONDITION		OUTPUT DATA	
MODE 1	MODE 0	OUTPUT DATA FORMAT	RATIO OF Y:U:V
L	L	Format 1	4:1:1
L	H	Format 2	4:4:4
H	L	Format 3	4:2:2
H	H	Not used	N/A

output data format (continued)

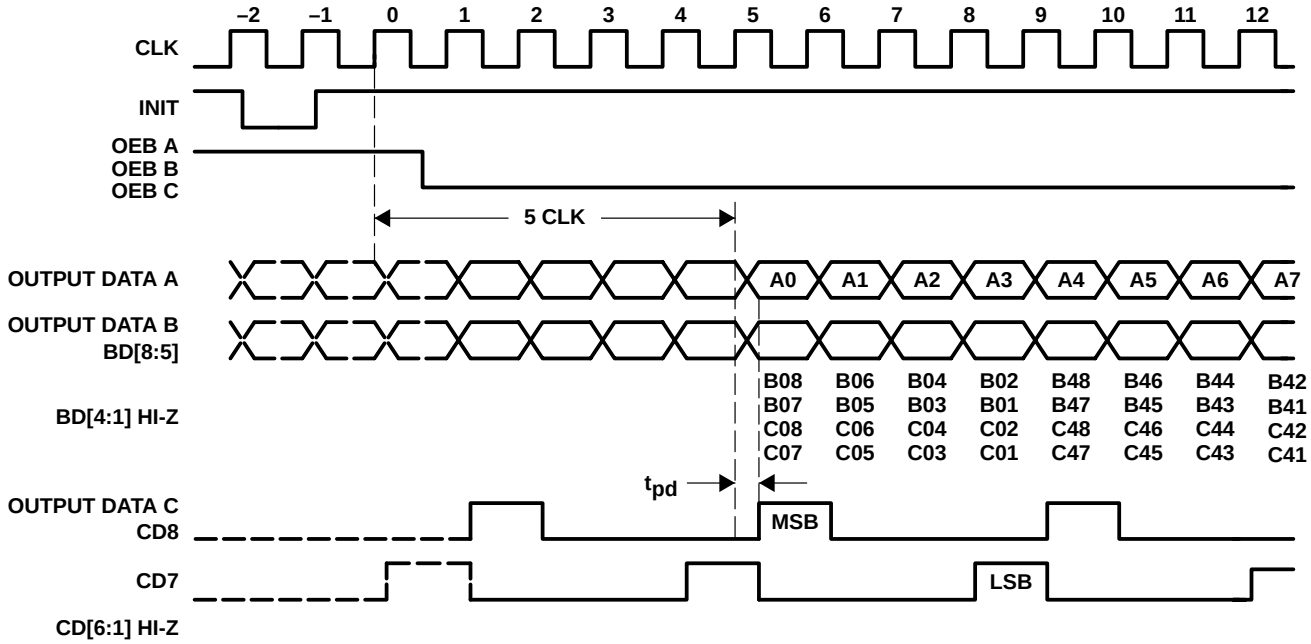


Figure 4. Format 1 (4:1:1) Timing Diagram

Table 5. Output Format 1 (4:1:1)

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK†							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B06	B04	B02	B48	B46	B44	B42
	BD7	B07	B05	B03	B01	B47	B45	B43	B41
	BD6	C08	C06	C04	C02	C48	C46	C44	C42
	BD5	C07	C05	C03	C01	C47	C45	C43	C41
	BD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
C	CD8	H	L	L	L	H	L	L	L
	CD7	L	L	L	H	L	L	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

† The first ADC sampling clock is denoted as CLK 0.
A06 is an example entry in the table where A shows the ADC channel, 0 represents the sampling order, and 6 is the bit number.

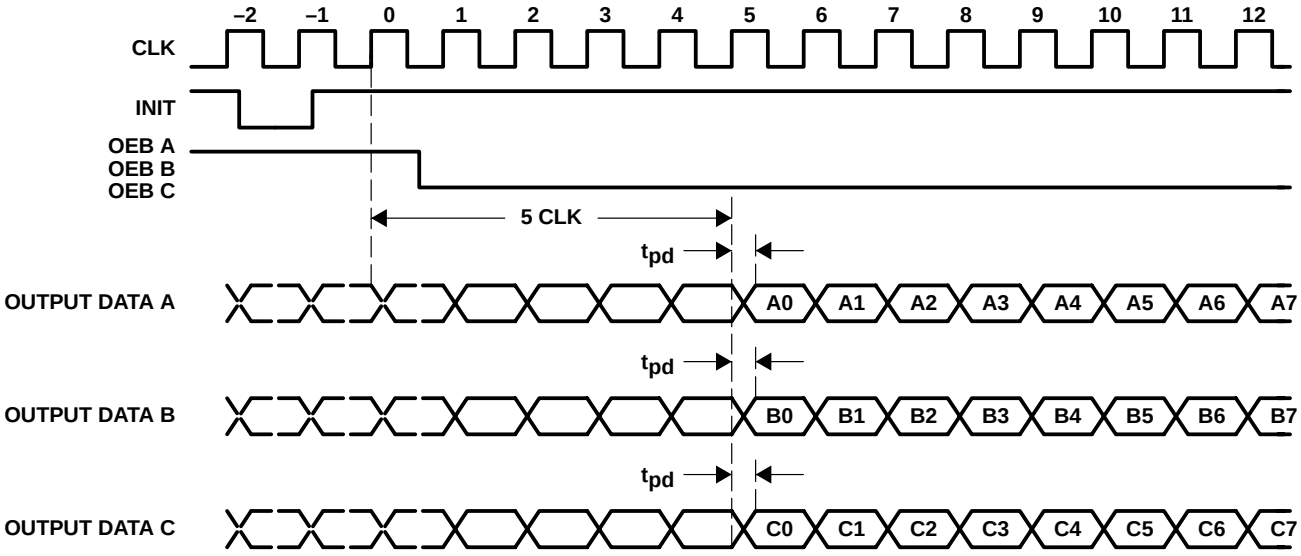


Figure 5. Format 2 (4:4:4) Timing Diagram

Table 6. Output Format 2 (4:4:4)

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK†							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B18	B28	B38	B48	B58	B68	B78
	BD7	B07	B17	B27	B37	B47	B57	B67	B77
	BD6	B06	B16	B26	B36	B46	B56	B66	B76
	BD5	B05	B15	B25	B35	B45	B55	B65	B75
	BD4	B04	B14	B24	B34	B44	B54	B64	B74
	BD3	B03	B13	B23	B33	B43	B53	B63	B73
	BD2	B02	B12	B22	B32	B42	B52	B62	B72
	BD1	B01	B11	B21	B31	B41	B51	B61	B71
C	CD8	C08	C18	C28	C38	C48	C58	C68	C78
	CD7	C07	C17	C27	C37	C47	C57	C67	C77
	CD6	C06	C16	C26	C36	C46	C56	C66	C76
	CD5	C05	C15	C25	C35	C45	C55	C65	C75
	CD4	C04	C14	C24	C34	C44	C54	C64	C74
	CD3	C03	C13	C23	C33	C43	C53	C63	C73
	CD2	C02	C12	C22	C32	C42	C52	C62	C72
	CD1	C01	C11	C21	C31	C41	C51	C61	C71

† The first ADC sampling clock is denoted as CLK 0.
A06 is an example entry in the table where A shows the ADC channel, 0 represents the sampling order, and 6 is the bit number.

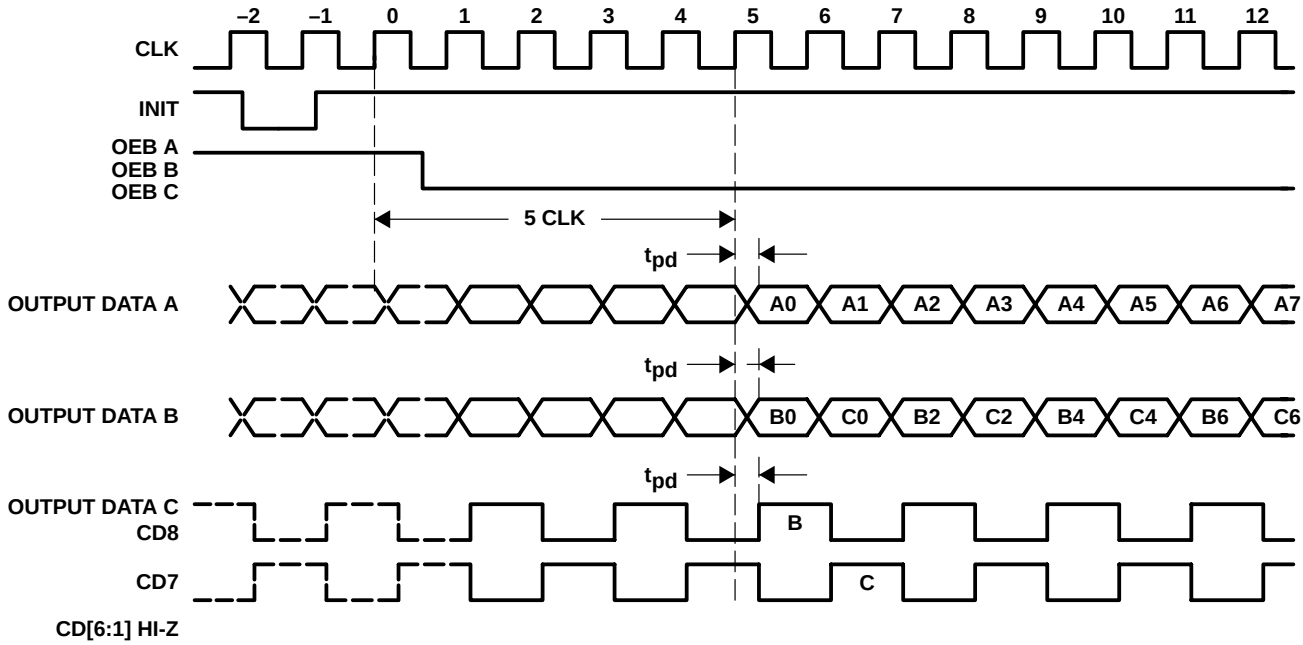


Figure 6. Format 3 (4:2:2) Timing Diagram

Table 7. Output Format 3 (4:2:2)

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK†							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	C08	B28	C28	B48	C48	B68	C68
	BD7	B07	C07	B27	C27	B47	C47	B67	C67
	BD6	B06	C06	B26	C26	B46	C46	B66	C66
	BD5	B05	C05	B25	C25	B45	C45	B65	C65
	BD4	B04	C04	B24	C24	B44	C44	B64	C64
	BD3	B03	C03	B23	C23	B43	C43	B63	C63
	BD2	B02	C02	B22	C22	B42	C42	B62	C62
	BD1	B01	C01	B21	C21	B41	C41	B61	C61
C	CD8	H	L	H	L	H	L	H	L
	CD7	L	H	L	H	L	H	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

† The first ADC sampling clock is denoted as CLK 0.
A06 is an example entry in the table where A shows the ADC channel, 0 represents the sampling order, and 6 is the bit number.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}‡ , V_{DD}§ . . . . . –0.3 V to 3.6 V
Reference voltage input range: $V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$, $V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$ . . . . . –0.3 V to V_{CC} +0.3 V
Analog input voltage range . . . . . –0.3 V to V_{CC} +0.3 V
Digital input voltage range, V_I . . . . . –0.3 V to 3.6 V
Digital output voltage range, V_O . . . . . –0.3 V to V_{CC} +0.3 V
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ V_{CC} refers to all analog supplies: A AV_{CC}, B AV_{CC}, and C AV_{CC}.
§ V_{DD} refers to all digital supplies: DV_{DD}, QA DV_{DD}, QB DV_{DD}, and QC DV_{DD}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage¶	(Analog) V_{CC}	3	3.3	3.6	V
	(Digital) V_{DD}	3	3.3	3.6	
Reference input voltage	$V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$	1.8	2	2.2	V
	$V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$	0.8	1	1.2	
$V_{ref(RT\ A)} - V_{ref(RB\ A)}$, $V_{ref(RT\ B)} - V_{ref(RB\ B)}$, $V_{ref(RT\ C)} - V_{ref(RB\ C)}$				1	V
High-level digital input voltage, V_{IH}		2			V
Low-level digital input voltage, V_{IL}				0.8	V
High-level pulse duration, $t_{w(H)}$ (at 50% of amplitude level)			16.7		ns
Low-level pulse duration, $t_{w(L)}$ (at 50% of amplitude level)			16.7		ns
Setup time for INIT input, t_{su}		3			ns
Hold time for INIT input, t_h		0			
Reset time for INIT input, t_{reset}		33.3			ns
Operating free-air temperature, T_A		–20		75	°C

¶ Within the electrical and operating characteristics table, when the term V_{DD} is used, DV_{DD} and all X DV_{DD} terminals are tied together, and when the term V_{CC} is used, all X AV_{CC} terminals are tied together.

electrical characteristics at V_{DD} = V_{CC} = 3.3 V, $V_{ref(RT)}$ = 2.0 V, $V_{ref(RB)}$ = 1.0 V, f(CLK) = 30 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clamp level accuracy			±0.5	±1	LSB
R_{REF}	Reference resistance	Measured between RT and RB		450		Ω
C_I	Analog input capacitance			5		pF
I_{IH}	High-level digital input current	V_{IH} = V_{DD} + 0.3 V			10	µA
I_{IL}	Low-level digital input current	V_{IL} = 0 V			10	µA
V_{OH}	High-level digital output voltage	V_{DD} = 3 V to 3.6 V, I_{OH} = –50 µA	V_{DD}–0.7			V
V_{OL}	Low-level digital output voltage	V_{DD} = 3 V to 3.6 V, I_{OL} = 50 µA			0.5	V
$I_{OH(lkg)}$	High-level digital output leakage current	OEB A = OEB B = OEB C = HI, V_{OH} = V_{DD}			10	µA
$I_{OL(lkg)}$	Low-level digital output leakage current	OEB A = OEB B = OEB C = HI, V_{OL} = 0 V			10	µA
	Supply current	f_S = 30 MSPS, NTSC ramp wave input	73	82	91	mA
	Power dissipation	f_S = 30 MSPS, NTSC ramp wave input	240	270	300	mW

operating characteristics V_{DD} = V_{CC} = 3.3 V, $V_{ref(RT)}$ = 2.0 V, $V_{ref(RB)}$ = 1.0 V, f(CLK) = 30 MHz, T_A = –20°C to 75°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNL	Differential nonlinearity	f_S = 30 MSPS		±0.2	±0.5	LSB
INL	Integral nonlinearity	f_S = 30 MSPS		±0.3	±0.75	LSB
f_S	Maximum conversion rate		30			MSPS
BW	Analog input bandwidth	At –3 dB, T_A = 25°C		130		MHz
t_{pd}	Digital output delay time	C_L = 10 pF (by design)			18	ns
	Zero-scale error	V_{ref} = REFT – REFB = 1 V	–16	–2	15	mV
	Full-scale error	V_{ref} = REFT – REFB = 1 V	–13	2	17	mV
	Sampling delay time	By design		4.3		ns

TYPICAL CHARACTERISTICS

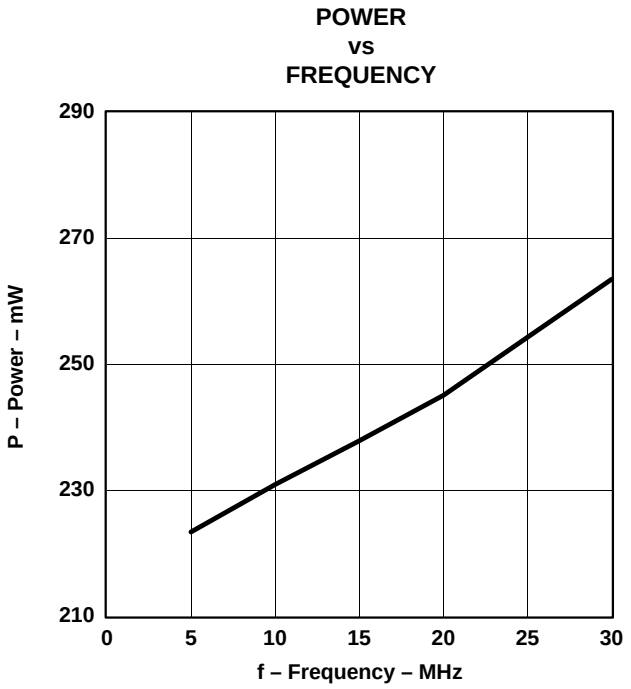


Figure 7

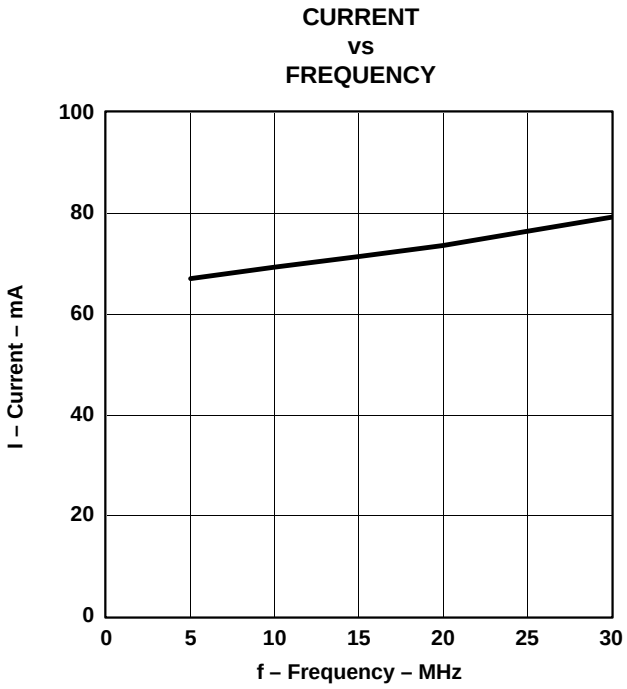


Figure 8

TYPICAL CHARACTERISTICS

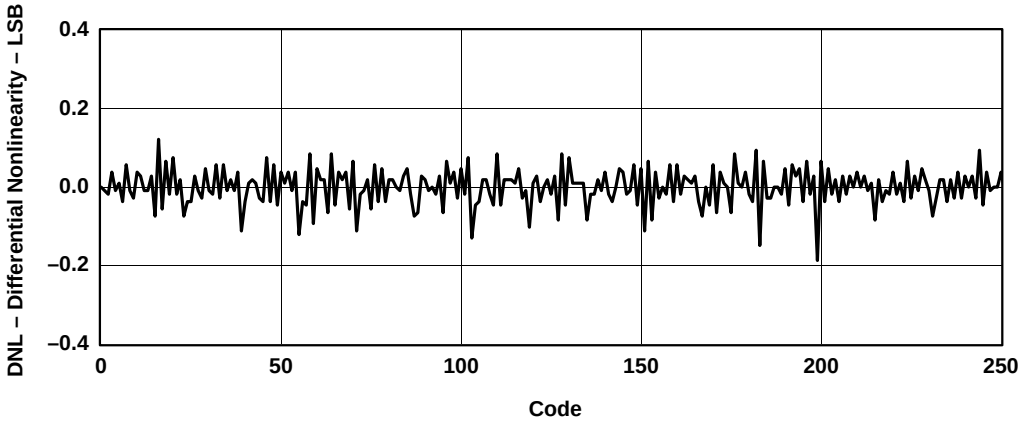


Figure 9. Typical Differential Nonlinearity, Channel A

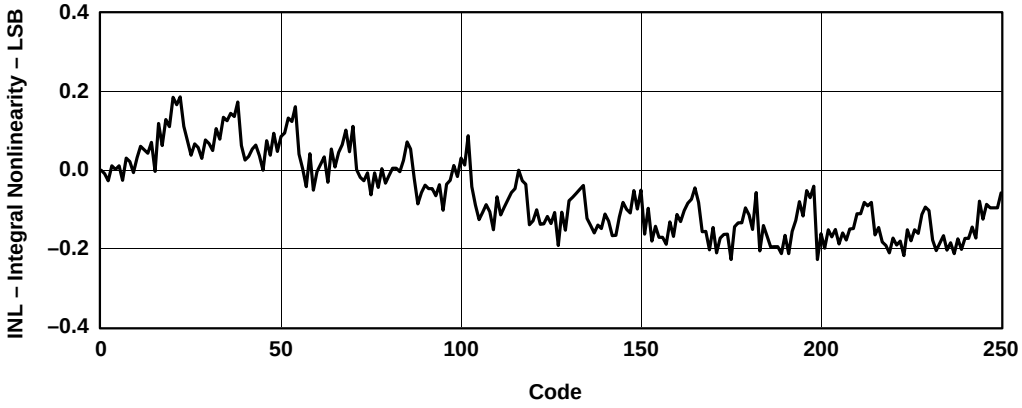


Figure 10. Typical Integral Nonlinearity, Channel A

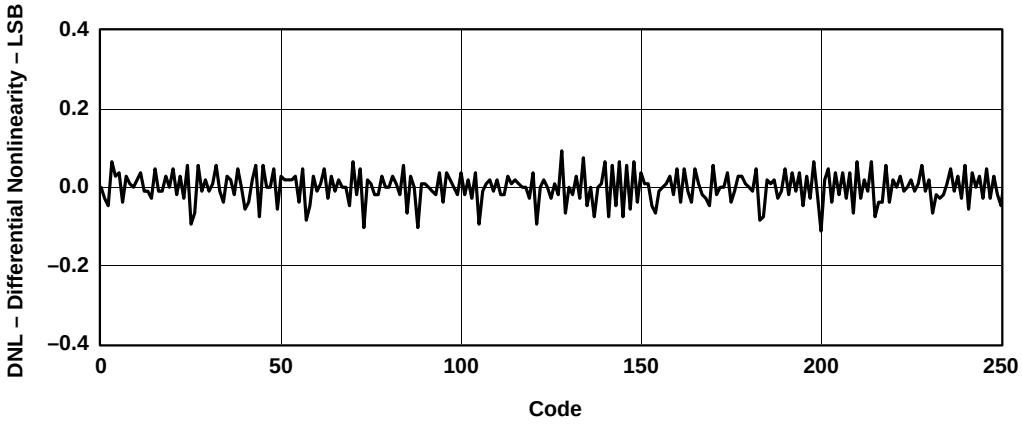


Figure 11. Typical Differential Nonlinearity, Channel B

TYPICAL CHARACTERISTICS

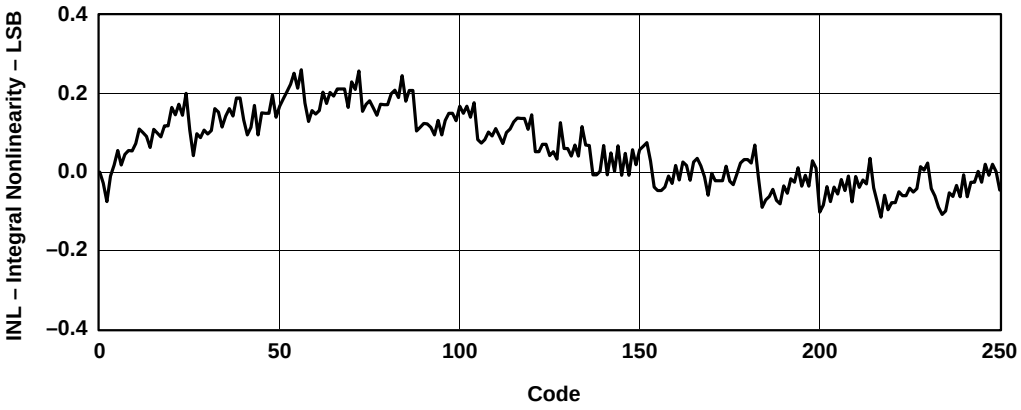


Figure 12. Typical Integral Nonlinearity, Channel B

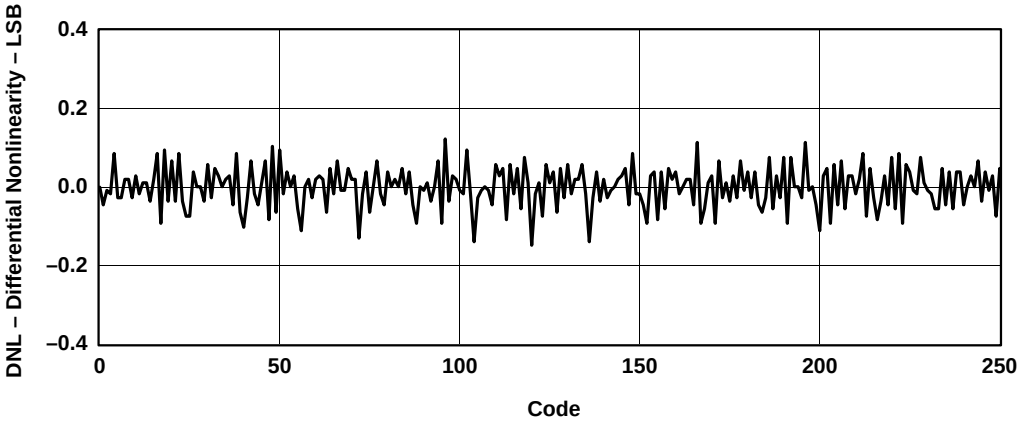


Figure 13. Typical Differential Nonlinearity, Channel C

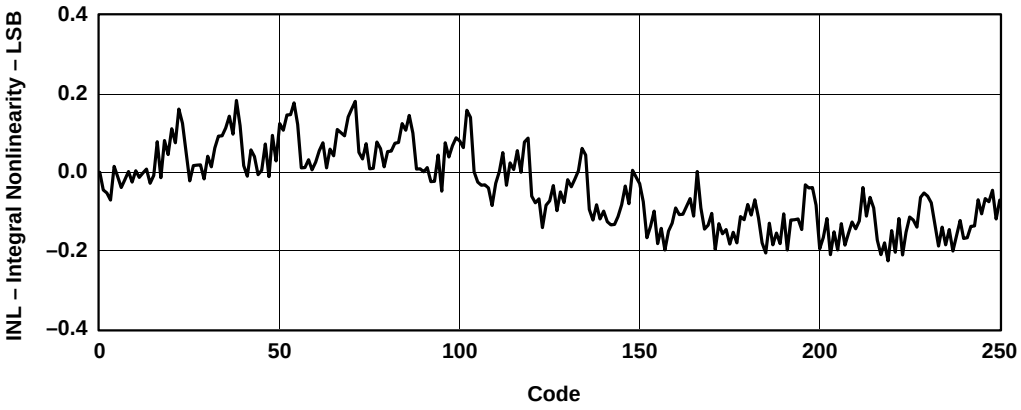
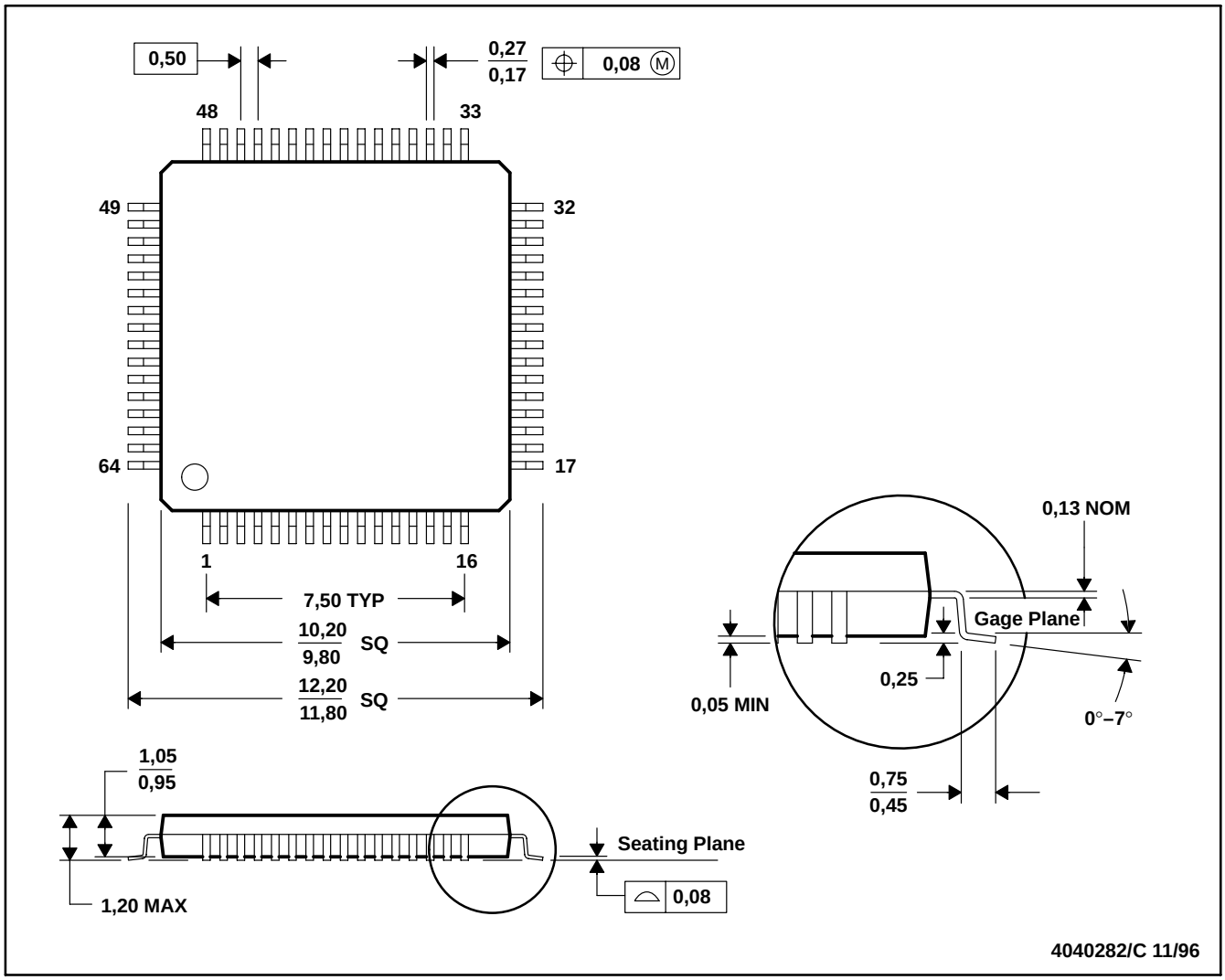


Figure 14. Typical Integral Nonlinearity, Channel C

MECHANICAL DATA

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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